#46
03/18/03

S/N 08/650,719 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner: Hong Kim
Serial No.:	08/650,719	Group Art Unit: 2187
Filed:	May 20, 1996	Docket: 303.623US1
Title:	ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION	

RESPONSE UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

This response is timely filed in reply to the Office Action mailed on November 27, 2002. Please consider the appended remarks rendered in **Appeal Brief Format**.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are four appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. These related appeals are currently pending before the Board and concern U.S. Patent Application Serial Number 08/984,560 (Atty. Ref:303.623US2), U.S. Patent Application Serial Number 08/984,561 (Atty. Ref:303.623US6), U.S. Patent Application Serial Number 08/984,562 (Atty. Ref:303.623US3), and U.S. Patent Application Serial Number 08/984,701 (Atty. Ref:303.623US5).

3. STATUS OF THE CLAIMS

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are currently pending, and the rejection of these claims is appealed. A clean copy of the pending claims is included as Appendix I.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Supplemental Response to the Second Final Office Action mailed to the Appellants on March 15, 2002, in which claim 7 was amended to correct a typographical error.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, embodiments of the invention disclosed relate to a memory device that selectably operates in either burst or pipelined modes. In one embodiment, an asynchronously addressable storage device 100 (Application, FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Application, Pg. 29, lines 5-25).

Some embodiments of the invention can switch between burst access and pipelined modes of operation without ceasing ("on the fly"). (Application, Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is used to select data within the device 100. A counter 149 included in the circuitry 122 increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses only external addresses 115 to access data within the device 100. (Application, Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited,

and accesses to memory may overlap without conflicting. (Application, Pg. 8, lines 1-5). In addition to the embodiments described, other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits are discussed. (Application, Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

1) Whether claim 61 was properly rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

2) Whether claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning (hereinafter "Manning").

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears,*

Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

b) The Reference

Manning: teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of the structure of the architecture, how it is applied, or its operation, are given.

c) Discussion of the Rejections

***c.1* -- The rejection under § 112**

Claim 61 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Because the elements of claim 61 were indeed described in the Application at the time of filing, the Appellants respectfully traverse this rejection.

The assertion was made "that 'selecting a pipelined mode of operation; proving [sic] a new external address for every [sic] associated with — while in a burst mode of operation; providing an initial external address associated — in the pipelined mode of operation; and while

in the burst mode of operation, generating at lest [sic] one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation' was not described in the specification." However, each of these elements is in fact described in several places in the Application as filed.

For example "selecting a pipelined mode of operation" is taught at pg. 29, lines 1, and 8-9, among numerous others. "Providing a new external address for every access associated with asynchronously accessing the ... device while in a burst mode of operation" is discussed at pg. 35, lines 8-10 and pg. 36, lines 9-10. "Switching modes to a burst mode of operation" is disclosed at pg. 30, lines 1-3 and 24-25, among numerous others. "Providing an initial external address associated with asynchronously accessing the ... device in the pipelined mode of operation" is noted at FIG. 15, time 210 and pg. 36, lines 14-15. Finally, "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation" is shown at pg. 27, lines 1-11; pg. 38, lines 11-15; and pg. 39, lines 9-16. It is respectfully noted that these same observations were made by the Appellants in a previous Response, however they may not have been noted by the Examiner since no mention was made of this in the most recent Office Action. Rather, the rejection appears to have simply been repeated, verbatim. Thus, since each of the elements of claim 61 were indeed disclosed in the Application at the time of filing, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

***c.2* -- The rejection under § 102**

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were rejected under 35 USC § 102(e) as being anticipated by Manning. First, the Applicants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Applicants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64. Therefore, the Applicants respectfully traverse this rejection under 35 USC § 102(e).

c.2.1. Why the reference does not disclose each and every element of the claimed

subject matter as arranged in the claims.

Manning specifically fails to disclose "circuitry ... configured to switch between the pipelined mode and the burst mode" as claimed by the Applicants in claim 1. Similarly, Manning fails to disclose that the burst mode and the pipelined mode are "extended data out modes" (claims 2-4); or that the "pipelined/burst mode circuitry" includes: a "buffer for storing an (external) address", a "counter for incrementing an address", "is coupled for receiving an external address", or"multiplexed devices for providing an internally generated address" (claims 5-9).

Further, Manning does not teach "selecting between" a "burst mode ... and" a "pipelined mode", or switching between such modes (claims 33-34, 46, 59-61); much less how addresses are supplied while selecting or switching modes (claim 35), or what type of switching environment may be used in burst and pipelined modes of operation (claims 48-49). Finally, Manning does not describe a system including a microprocessor and memory "selectively operable either in a burst mode or a pipelined mode", or a storage device/memory including circuitry "switchable between burst and pipeline modes of operation" (claims 50, and 63-64).

Several assertions were made which attribute support to various concepts allegedly disclosed by Manning in the Office Action. However, a careful reading of each citation reveals that the discussion of the asserted elements is either vague, nonexistent, or completely in error. These assertions have been made with respect to:

Claims 2, 3 - Manning does not disclose that the pipelined mode is an EDO mode of operation (the two concepts are never discussed in conjunction with each other).

Claim 9 - Manning does not disclose mode selection circuitry which includes a multiplexed device (the components referenced in the Office Action are an address counter 26 and a column address decoder 30).

Claim 34 - Manning does not disclose *switching* between the pipelined mode and the burst mode (Manning merely refers to the possibility of using a pipelined *architecture*).

Claim 35 - Manning does not disclose selecting an external address along with *selecting*

between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 48, 49 - Manning does not disclose several switching environments in conjunction with burst and pipelined modes (Manning merely refers to the possibility of using a pipelined *architecture*).

Two more erroneous assertions are directed toward all pending claims. First, it is not true that one must "select pipeline mode" to "work in the pipeline architecture" (See Paper 40, page 7 - the assertion is erroneous because the pipelined mode does not need to be selected if a device always operates in that mode). Second, in contrast to assertions tendered by the Office, the feature of switching between pipelined and burst mode operations in the same memory are included in each of the rejected claims, since each claim is directed toward a single device, accessing a single device, accessing different locations in a single device, or a single device included in a system.

c.2.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Applicants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and pipelined modes of operation, as claimed in claims 1, 33, 34, 46, 50, 59, 60, 61, 63, and 64 (and in all claims that depend from them)?

Second, the Office has failed to produce a *prima facie* case of anticipation. While the assertion is made that Manning discloses "mode circuitry to select between a burst mode and a pipelined mode", and that the circuitry is "configurable to select between [the] two modes", the Applicants' representative, after a careful study of Manning, was unable to locate any such selection circuitry, nor any aspect of such circuitry which was configurable to select between

burst and pipelined modes of operation.

For example, the only references offered by the Office to support the assertion that Manning "discloses the invention as claimed" with respect to claim 1 are: Fig.1, Ref. 40; col. 5, lines 41-50; col. 6, lines 14-34; and col 7, lines 43-54. Fig. 1, Ref. 40 is a block "mode register", with no indication regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 41-50 discuss the possibility of using a pipelined architecture (e.g., perhaps this refers to a pipelined *output* stage of a burst EDO device? see below ...), but not as enabling switching between true pipeline mode or burst mode access operations, as disclosed and claimed by the Applicants. Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, as claimed by the Applicants in independent claim 1, as well as in independent claims 33, 46, 50, 59-61, 63, and 64, and all of the claims which depend from them.

Third, the Applicants respectfully draw attention to a statement in the Office Action (Paper 40, page 7) that claim 1 reads on "switching between standard fast page mode (non-EDO) and burst mode". The Applicants' representative was unable to find any portion of Manning to support the idea that the fast page mode of operation is the same as a pipelined mode of operation, and no support has been provided by the Office in response to repeated requests by the Applicants that such support for this proposition in Manning be designated with specificity.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as part of

Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory further improved EDO performance by adding **a pipeline stage** (i.e., **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined

by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

In embodiments of the Appellants' invention, a newburst signal from control logic is described. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with an initial external address stored in a temporal storage device. Consequently, if burst operation is the selected mode of operation, then a counter is used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through a memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13)

In short, what is discussed by Manning is not identical to the subject matter of various embodiments of the invention as required by the M.P.E.P., and therefore, the rejection is under § 102 is improper. Reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

c.3 Why the claims are separately patentable:

While the separate patentability of each claim has been discussed in the "Argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 1 is directed toward an asynchronously-accessible storage device having "mode circuitry configured to switch between a burst mode and a pipelined mode" and "circuitry operable in either a burst mode or pipelined mode ... for operating the asynchronously-accessible storage device in either mode." Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 1, dependent claim 2 adds "the burst mode and the pipelined mode are extended data out modes of operation." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 3 adds "the pipelined mode is an extended data out mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 4 adds "the burst mode is an extended data out mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 5 adds "the pipelined ... mode circuitry includes a buffer ... for storing an address." Manning does not disclose this combination of elements, and no other claim (except claim 6) has this unique combination of elements. To the elements of dependent claim 5, dependent claim 6 adds "the pipelined ... mode circuitry includes at least one counter ... for incrementing the address." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 7 adds "the pipelined ... mode circuitry is coupled for reading an external address." Manning does not disclose this combination of elements, and no other claim (except claims 8 and 9) has this unique combination of elements. To the elements of dependent claim 7, dependent claim 8 adds "the pipelined ... mode circuitry includes a buffer ... for storing the external address." To the elements of dependent claim 7, dependent claim 9 adds "the pipelined ... mode circuitry includes multiplexed

devices for providing an internally generated address to the storage device." Manning does not disclose these combinations of elements, and no other claims have these unique combinations of elements.

Independent claim 33 is directed toward a method of accessing a storage device comprising "receiving a first address", "obtaining a second address", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode" and "asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address." Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 33, dependent claim 34 adds "switching between the burst mode and the pipelined mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 33, dependent claim 35 adds "the second address is an external address." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 46 is directed toward a method of accessing a storage device comprising "selecting a pipelined mode of operation", "providing a new external address for every access associated with asynchronously accessing the ... device while in the pipelined mode of operation", and "switching modes to a burst mode of operation". Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 46, dependent claim 48 adds "the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 46, dependent claim 49 adds "the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 50 is directed toward a system including "a microprocessor" and "a memory coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory". Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

Independent claim 59 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal", and "accessing a storage element ... in the selected mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 60 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between outputting information ... and inputting information", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal" and "asynchronously accessing a storage element ... in the selected mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 61 is directed toward a method of accessing a storage device comprising "selecting a pipeline mode of operation", "providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation", "switching modes to the burst mode of operation", and

"while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 63 is directed toward a storage device having "an array of memory cells" and "mode circuitry for receiving a burst/pipeline signal". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 64 is directed toward a memory circuit having "an array of memory cells" and "burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

c.4 **-- The double patenting rejection:**

Claims 59 and 60 were provisionally rejected under the judicially created doctrine of double patenting over claim 36 of co-pending Application No. 08/984,563. Claim 61 was provisionally rejected under the judicially created doctrine of double patenting over claim 59 of co-pending Application No. 08/984,561.

Co-pending U.S. Patent Application Serial Nos. 08/984,563 and 08/984,561 have not yet received any final indication of allowed claims. The Applicants request that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending applications to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

9. SUMMARY

It is respectfully submitted that claim 61 is indeed supported by the subject matter contained in the Application as-filed, and that a case of anticipation under 35 U.S.C. §102 has not been established. Therefore, reconsideration and withdrawal of the rejections of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

The Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicants' attorney, **Mark Muller at (210) 308-5677**, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 27 Feb 2003 By _____

Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner of Patents, Washington, D.C. 20231, on this 27 day of January, 2003.

Tina Kohout
Name

_____
Signature